What is claimed is:

1. A semiconductor memory device in which one bit memory cell is composed of one transistor, wherein the transistor comprises:

a semiconductor layer which is a first conduction type and electrically isolated from other memory cells to get floating;

a drain diffusion region which is a second conduction type, formed in the first conduction-type semiconductor layer, and connected to a bit line;

a source diffusion region which is the second conduction type, formed apart from the drain diffusion region in the first conduction-type semiconductor layer, and connected to a source line; and

a gate electrode which is formed on the semiconductor layer between the drain diffusion region and the source diffusion region with a gate insulator therebetween, and connected to a word line;

wherein the transistor has a first data state having a first threshold voltage in which excessive majority carriers are held in the semiconductor layer and a second data state having a second threshold voltage in which the excessive majority carriers in the semiconductor layer are emitted.

2. The semiconductor memory device according to claim 1,

wherein the first data state is a state in which impact ionization is generated near a drain junction by operating the transistor and in which excessive majority carriers produced by this impact ionization are held in the semiconductor layer, and

the second data state is a state in which a forward bias is applied between the semiconductor layer and the drain diffusion region to extract the excessive majority carriers from within the semiconductor layer to the drain diffusion region.

3. The semiconductor memory device according to claim 1, wherein the semiconductor layer is a silicon layer formed on a silicon substrate with an insulating film therebetween.

4. The semiconductor memory device according to claim 3,

wherein the silicon layer is a p-type, and the transistor is an N-channel MOS transistor.

5. The semiconductor memory device according to claim 1, wherein a voltage of the source line is constant.

6. The semiconductor memory device according to claim 5, wherein when data is written,

with the source line as a reference voltage,

a first voltage higher than the reference voltage is given to a word line of a selected transistor,

a second voltage lower than the reference voltage is given to a word line of a non-selected transistor,

a third voltage higher than the reference voltage is given to the bit line when the first data state is written, and a fourth voltage lower than the reference voltage is given to the bit line when the second data state is written.

7. The semiconductor memory device according to claim 6, wherein when the data is read,

with the source line as the reference voltage,

a fifth voltage, which is between the first threshold voltage and the second threshold voltage and higher than the reference voltage, is given to the word line of the selected transistor to detect conduction/non-conduction of the selected transistor.

8. The semiconductor memory device according to claim 6, wherein when the data is read,

with the source line as the reference voltage,

a fifth voltage, which is higher the first and second threshold voltages and higher than the reference voltage, is given to the word line of the selected transistor to detect a conductivity of the selected transistor.

9. The semiconductor memory device according to claim 1, wherein the semiconductor layer comprises:

a first impurity region being in contact with the drain

diffusion region and the source diffusion region; and

a second impurity region disposed apart from the drain diffusion region and the source diffusion region, being in contact with the first impurity region and having an impurity concentration higher than the first impurity region.

10. The semiconductor memory device according to claim 9, wherein at least the drain diffusion region out of the drain diffusion region and the source diffusion region comprises:

a third impurity region being in contact with the first impurity region to compose a pn junction; and

a fourth impurity region formed apart from the first impurity region and having an impurity concentration higher than the third impurity region.

11. A semiconductor memory device comprising:

an SOI substrate in which a silicon layer is formed on an insulating film formed on a silicon substrate;

a plurality of transistors formed in the silicon layer, pairs of transistors, each pair sharing a drain diffusion region, being arranged in a matrix form with element-isolated in a channel width direction;

a plurality of word lines each connected to gate electrodes of transistors arranged in a first direction in common;

a plurality of bit lines disposed in a second direction intersecting the first direction and connected to the drain diffusion regions of the transistors;

a common source line formed by continuously disposing source diffusion regions of the transistors arranged in the first direction,

wherein the transistor has a first data state having a first threshold voltage in which excessive majority carriers are held in the silicon layer and a second data state having a second threshold voltage in which the excessive majority carriers in the silicon layer are emitted.

12. The semiconductor memory device according to claim 11,

wherein the transistors, each having a cell size of 2F × 2F where F is a minimum feature size, are arranged in a matrix form.

13. The semiconductor memory device according to claim 11, wherein the drain diffusion region and the source diffusion region are formed deep to reach the insulating film located under the silicon layer.

14. The semiconductor memory device according to claim 11,

wherein the first data state is a state in which impact ionization is generated near a drain junction by operating the transistor and in which excessive majority carriers produced by this impact ionization are held in the silicon layer, and

the second data state is a state in which a forward bias is applied between the silicon layer and the drain diffusion region to extract the excessive majority carriers from within the silicon layer to the drain diffusion region.

15. The semiconductor memory device according to claim 14, wherein the silicon layer is a p-type, and the transistor is an N-channel MOS transistor.

16. The semiconductor memory device according to claim 11, wherein a voltage of the common source line is constant.

17. The semiconductor memory device according to claim 16, wherein when data is written,

with the common source line as a reference voltage,

a first voltage higher than the reference voltage is given to a word line of the selected transistor,

a second voltage lower than the reference voltage is given to a word line of the non-selected transistor,

a third voltage higher than the reference voltage is given to the bit line when the first data state is written, and a fourth voltage lower than the reference voltage is given to the bit line when the second data state is written.

18. The semiconductor memory device according to claim 16, wherein when the data is read,

with the common source line as the reference voltage,

a fifth voltage, which is between the first threshold voltage and the second threshold voltage and higher than the reference voltage, is given to the word line of the selected transistor to detect conduction/non-conduction of the selected transistor.

19. The semiconductor memory device according to claim 16, wherein when the data is read,

with the common source line as the reference voltage,

a fifth voltage, which is higher the first and second threshold voltages and higher than the reference voltage, is given to the word line of the selected transistor to detect a conductivity of the selected transistor.

20. A method of manufacturing a semiconductor memory device, comprising:

forming an insulating film on a semiconductor substrate;

forming a first conduction-type semiconductor layer on the insulating film;

forming a mask having an opening in a gate forming region on the semiconductor layer;

forming a side wall insulating film on a side wall of the opening of the mask;

doping impurities to the semiconductor layer through the opening of the mask to form a first conduction-type impurity region having an impurity concentration higher than the semiconductor layer;

forming a gate insulator and a gate electrode by burying them in the opening of the mask after the side wall insulating film is removed; and

doping impurities to the semiconductor layer to form second conduction-type drain diffusion region and source diffusion region after the mask is removed.

21. A method of manufacturing a semiconductor memory device,

comprising:

forming an insulating film on a semiconductor substrate;

forming a first conduction-type semiconductor layer on the insulating film;

forming a mask having an opening in a gate forming region on the semiconductor layer;

forming a first side wall insulating film on a side wall of the opening of the mask;

doping impurities to the semiconductor layer through the opening of the mask to form a first conduction-type first impurity region having an impurity concentration higher than the semiconductor layer;

forming a gate insulator and a gate electrode by burying them in the opening of the mask after the first side wall insulating film is removed;

doping impurities to the semiconductor layer to form second conduction-type second impurity regions in a drain region and a source region after the mask is removed,

forming a second side wall insulating film on a side wall of the gate electrode, and

doping impurities to the semiconductor layer to form second conduction-type third impurity regions having an impurity concentration higher than the second impurity regions in the drain region and the source region.